

100Gb/s CFP2 Optical Transceiver

R M290-601



Features

- **D LC**
- **+3.3**
- **H -**
- **O 112G**
- **10**
- **AC CML**
- **1310 EA-DFB LD**
- **PIN RO A**
- **L (M :9)**
- **B**
- **O :0℃ 70℃**
- **C R H**
- **MDIO C I**

Application

- **O N-O 4**
-
-
- **P P A N**

Standards

- C IEEE 802.3
- C CFP2 M A , 1.0 J
- 31,2014
- C CFP M A , 2.2J
- 01, 2013
- C I - G.959.1
- C R H & EEE

Absolute Maximum Ratings

Parameter	Symbol	Unit	Min	Max
Storage Temperature Range	Ts	°C	-40	+85
Relative Humidity	RH	%	5	85

Output Low Voltage ($I_{OL}=100\mu A$)	3.3VOL	V	0.2		
Minimum Pulse Width of Control Pin Signal	t_CNTL	us	100		
1.2V LVCMOS Electrical Characteristics					
Input High Voltage	1.2VIH	V	0.84	1.5	
Input Low Voltage	1.2VIL	V	-0.3	0.36	
Input Leakage Current	1.2IIN	uA	-100	+100	
Output High Voltage	1.2VOH	V	1.0	1.5	
Output Low Voltage	1.2VOL	V	-0.3	0.2	
Output High Current	1.2IOH	mA	-4		
Output Low Current	1.2IOL	mA	+4		
Input Capacitance	Ci	pF	10		
Optical transmitter Characteristics					
Signaling Rate for Each Lane (100GbE)	Gbps		-	25.78125	
27.95249					
Four Lane Wavelength Range	λ_1	nm	1294.53	1295.56	1296.59
	λ_2		1299.02	1300.05	1301.09
	λ_3		1303.54	1304.58	1305.63
	λ_4		1308.09	1309.14	1310.19
Side Mode Suppression Ratio	SMSR	dB	30	-	
Total Average Launch Power	Pt	dBm	-	10.5	
Average Launch Power for Each Lane(100GbE)	Pa	dBm	-4.3	+4.5	2
Average Launch Power for Each Lane(OTU4)			-2.9	+4.5	
Optical Modulation Amplitude for Each Lane	OMA	dBm	-1.3	4.5	3
Transmitter and Dispersion Penalty for Each Lanes	TDP		2.2		
Average Launch Power of Off Transmitter for Each Lanes	Poff	dBm	-	-30	
Extinction Ratio (100GbE)	EX	dB	4		
Extinction Ratio (OTU4)			7		
RIN_{20OMA}	dB/Hz		-130		
Optical Return Loss Tolerance	dB		20		
Transmitter Reflectance	dB		-12 4		
Eye Diagram	Compliant with IEEE 802.3ba-LR4/OTU4				
Optical receiver Characteristics					
Receive Rate for Each Lane(100GbE)	Gbps		-	25.78125	
27.95249					
Four Lane Wavelength Range	λ_1	nm	1294.53	1295.56	1296.59
	λ_2		1299.02	1300.05	1301.09
	λ_3		1303.54	1304.58	1305.63
	λ_4		1308.09	1309.14	1310.19
Overload Input Optical Power	Pmax	dBm	5.5	5	
Average Receive Power for Each Lane(100GbE)	Pin	dBm	-10.6	4.5	6&7
Average Receive Power for Each Lane(OTU4)			-9.2	4.5	
Receive Power In OMA for Each Lane	PinOMA	dBm	-	4.5	
Difference in Receive Power between Any Two Lanes	dBm		-	5.5	

Receiver Sensitivity in OMA for Each Lane(100GbE)	SOMA	dBm	-8.6	8
Receiver Sensitivity in OMA for Each Lane(OTU4)			-10.8	9
Stressed Receiver Sensitivity in OMA for Each Lane		dBm	-6.8	10&11
Los Assert		dBm		-12
Los De-assert		dBm	-17	
Los Hysteresis		dBm	0.2	

Note1. The supply current includes CFP module's supply current and test board working current.

Note2. Average launch power ,each lane(min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance

Note3.Even if the TDP<1dB, the OMA(min) must exceed this value

Note4.Transmitter reflectance is defined looking into the transmitter

Note5.The receiver shall be able to tolerate , without damage, continuous exposure to an optical input signal having this average power level

Note6.The average receive power , each lane (max) for 100GBASE-ER4 is larger than the 100BASE-ER4 transmitter value to allow compatibility with 100BASE-LR4 units at short distances

Note7.Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance

Note8.Receiver sensitivity (OMA), each lane (max) is informative

Note9. Measured withPRBS 2³¹-1 for BER=10⁻⁵. The BER for the OTU4 application is required to be met only after FEC has been applied.

Note10. Measured with conformance test signal at TP3 for BER=10⁻¹²

Note11. conditions of stressed receiver sensitivity test: vertical eye closure penalty for each lane is 1.8dB;stressed eye J2 jitter for each lane is 0.3UI; stressed eye J9 jitter for each lane is 0.47UI.

Hardware Control Pins

The CFP Module support real-time control functions via hardware pins, listed in the following table: Hardware Control Pins

Hardware Control Pins							
Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
11	TX_DIS (PRG_CNTL)	Transmitter Disable	I	3.3V LVCMOS	Disable	Enable	Pull-Up Note1
14	MOD_LOPWR	Module Low Power Mode	I	3.3V LVCMOS	Low Power	Enable	Pull-Up Note1
16	MOD_RSTn	Module Reset(Invert)	I	3.3V LVCMOS	Enable	Reset	Pull-Down Note2

Note1: Pull-Up resistor (4.7KOhm to 10 KOhm) is located within the CFP module

Note2: Pull-Down resistor (4.7KOhm to 10 kOhm) is located within the CFP module

Hardware Alarm Pins

The CFP Module supports alarm hardware pins listed in the following table: Hardware Alarm Pins

Hardware Alarm Pins							
Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
15	MOD_ABS	Module Absent	O	3.3V LVCMOS	Absent	Present	Pull-Down Note1
12	RX_LOS (PRG_ALARM)	Receiver Loss of Signal	O	3.3V LVCMOS	Loss of Signal	OK	

Note1: Pull-Down resistor (<100Ohm) is located within the CFP module. Pull-up should be located on the host

Management Interface Pins(MDIO)

The CFP Module supports alarm, control and monitor functions via an MDIO bus. The CFP MDIO pins are listed in the following table: Management Interface Pins

Management Interface Pins

Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
13	GLB_ALRMn	Global Alarm	I	3.3V LVCMOS	Ok	Alarm	
18	MDIO	Management Data Input Output Bi-Directional Data	I/O	1.2V LVCMOS			
17	MDC	MDIO Clock	I	1.2V LVCMOS			
19	PRTADR0	MDIO Physical Port address bit0	I	1.2V LVCMOS	per MDIO document[5]		
20	PRTADR1	MDIO Physical Port address bit1	I	1.2V LVCMOS			
21	PRTADR2	MDIO Physical Port address bit2	I	1.2V LVCMOS			

Hardware Signaling Pin Timing Requirements

Timing Parameters for CFP hardware Signal Pins are listed in the following table.

Timing Parameters for CFP hardware Signal Pins

Parameter	Symbol	Min	Max	Unit	Notes&Conditions
Hardware assert	MOD_LOPWR t_MOD_LOPWR_assert		1	ms	

Time					"OR" of Associated MDIO alarm& status registers.Please see MDIO document for further details
Global Alarm De-assert Delay Time	GLB_ALRMn_deassert		150	ms	This is a logical "OR" of Associated MDIO alarm& status registers.Please see MDIO document for further details
Management Interface Clock Period	t_prd	250		ns	MDC is 4MHz rate
Host MDIO t_setup	t_setup	10		ns	
Host MDIO t_hold	t_hold	10		ns	
CFP MDIO t_delay	t_delay	0	175	ns	
Initialization time from Reset	t_initialize		2.5	s	
Transmitter Disabled(TX_DIS_asserted)	t_deassert		100	us	Application Specific
Transmitter Enabled(TX_DIS_asserted)	t_assert		20	ms	Value is dependent upon module start-up time.Please See register "Maximum TX-Turn-on Time" in "CFP MSA Management Interface Specification"

High Speed Electrical Characteristics

Reference Clock Characteristics (optional)

		Min	Typ	Max	Unit	Notes
Impedance	Zd	80	100	120		

1/

161.1328125/644.53125

Frequency

MHz

Differential Voltage						Differential
RMS jitter ^{1,2}	σ			10	ps	Random Jitter Over frequency band of 10KHz<f<10MHz
Clock Duty Cycle		40		60	%	
Clock Rise/Fall Time 10%/90%	$t_{r/f}$	200		1250	ps	1/64 of electrical lane rate
		50		315		1/16 of electrical lane rate

Optional Transmitter and Receiver Monitor Clock Characteristics

Min Typ

				Network Lane		
801D	1	RO	7~0	Maximum Power Consumption		
801E	1	RO	7~0	Maximum Power Consumption in Low Power Mode		
801F	1	RO	7~0	Maximum Operating Case Temp Range		
8020	1	RO	7~0	Minimum Operating Case Temp Range		
8021	16	RO	7~0	Vendor Name		
8031	3	RO	7~0	Vendor OUI		
8034	16	RO	7~0	Vendor Part Number		
8044	16	RO	7~0	Vendor Serial Number		
8054	8	RO	7~0	Data Code		
805C	2	RO	7~0	Lot Code		
805E	10	RO	7~0	CLEI Code		
8068	1	RO	7~0	CFP MSA hardware Specification Revision Number		
8069	1	RO	7~0	CFP MSA Management Interface Specification Revision Number		
806A	2	RO	7~0	Module Hardware Version Number		
806C	2	RO	7~0	Module Firmware Version Number		
806E	1	RO	7~0	Digital Diagnostic Monitoring Type		
806F	1	RO	7~0	Digital Diagnostic Monitoring		
8075	1	RO	7~0	Heat Sink Type		
8076	1	RO	7~0	Maximum TX-Turn-off Time		

8084	
8086	
8088	
808A	
808C	
808E	
8090	
8092	
8094	
8096	
8098	
809A	
809C	
809E	
80A0	
80A2	
80A4	
80A6	
80A8	
80AA	
80AC	
80AE	

80B0	2	RO	7~0	Threshold			
------	---	----	-----	-----------	--	--	--

			Select			
			15~8	Reserved		
A008	1	RW	7~0	Function Select Code		
		RO		PRG_ALARM3Source Select		
			15~8	Reserved		
		RW	7~0	Alarm Source Code		
A009	1	RO		PRG_ALARM2Source Select		
			15~8	Reserved		
		RW	7~0	Alarm Source Code		
A00A	1	RO		PRG_ALARM1Source Select		
			15~8	Reserved		
		RW	7~0	Alarm Source Code		
A00B	1	RO		Module Bi-/Uni-Directional Operating Mode Select		
			15~3	Reserved		
		RW	2~0	Module Bi/uni-Direction Mode Select		
A00C	4	RO		Reserved		
Module Control Registers						
A010	1			Module General Control		
		RW/SC/LH	15	Soft Module Reset		
		RW	14	Soft Module Low Power		
		RW	13	Soft TX Disable		
		RW	12	Soft PRG_CNTL3 Control		
		RW	11	Soft PRG_CNTL2 Control		
		RW	10	Soft PRG_CNTL1 Control		
		RW	9	Soft GLB_ALARM Test		
		RO	8~6	Reserved		
		RO	5	TX_DIS Pin State		
		RO	4	MOD_LOPWR Pin State		
		RO	3	PRG_CNTL3 Pin State		
		RO	2	PRG_CNTL2 Pin State		
		RO	1	PRG_CNTL1 Pin State		
		RO	0	Reserved		
A011	1			Network Lane TX Control		
		RO	15	Reserved		
		RW	14	TX PRBS Generator Enable		
		RW	13	TX PRBS Pattern 1		
		RW	12	TX PRBS Pattern 0		
		RW	11	TX De-skew Enable		
		RW	10	TX FIFO Reset		
		RW	9	TX FIFO Auto Reset		
		RW	8	TX Reset		
		RW	7~5	TX MCLK Control		
		RO	4	Reserved		
		RW	3~1	TX Rate Select (10G lane rate)		
		RW	0	TX Reference CLK Rate Select		
A012	1			Network Lane RXControl		
		RW	15	Active Decision Voltageand Phase function		
		RW	14	RX PRBS CheckerEnable		
		RW	13	RX PRBS Pattern 1		
		RW	12	RX PRBS Pattern 0		
		RW	11			

			12	Network Lane Alarm and Warning Summary		
			11	Module Alarm and Warning 2 Summary		
			10	Module Alarm and Warning 1 Summary		
			9	Module Fault Summary		
			8	Module General Status Summary		
			7	Module State Summary		
			6~1	Reserved		
			0	Soft GLB_ALRM Test Status		
A019	1	RO		Network Lane Alarm and Warning Summary		
			15	Lane 15 Alarm and Warning Summary		
			14	Lane 14 Alarm and Warning Summary		
			13	Lane 13 Alarm and Warning Summary		
			12	Lane 12 Alarm and Warning Summary		
			11	Lane 11 Alarm and Warning Summary		
			10	Lane 10 Alarm and Warning Summary		
			9	Lane 9 Alarm and Warning Summary		
			8	Lane 8 Alarm and Warning Summary		
			7	Lane 7 Alarm and Warning Summary		
			6	Lane 6 Alarm and Warning Summary		
			5	Lane 5 Alarm and Warning Summary		
			4	Lane 4 Alarm and Warning Summary		
			3	Lane 3 Alarm and Warning Summary		
			2	Lane 2 Alarm and Warning Summary		
			1	Lane 1 Alarm and Warning Summary		
			0	Lane 0 Alarm and Warning Summary		
A01A	1	RO		Network Lane Fault and Status Summary		
			15	Lane 15 Fault and Status Summary		
			14	Lane 14 Fault and Status Summary		
			13	Lane 13 Fault and Status Summary		
			12	Lane 12 Fault and Status Summary		
			11	Lane 11 Fault and Status		

				Summary		
			10	Lane 10 Fault and Status Summary		

A01C	1	RO		Reserved		
Module FAWS Registers						
A01D	1	RO		Module General Status		
			15	Reserved		
			14	Reserved		
			13	HW_Interlock		
			12~11	Reserved		
			10	Loss of REFCLK Input		
			9	TX_JITTER_PLL_LOL		

		RO/LH/COR RO/LH/COR	7	TX-Turn-off State Latch		
--	--	------------------------	---	-------------------------	--	--

		RO/LH/COR	3	Mod Aux 2 High Alarm Latch		
		RO/LH/COR	2	Mod Aux 2 High Warning Latch		
		RO/LH/COR	1	Mod Aux 2 Low Warning Latch		
		RO/LH/COR	0	Mod Aux 2 Low Alarm Latch		
A027	1	RO		Reserved		
A028	1			Module Stable Enable		
		RO	15~9	Reserved		
		RW	8	High-Power-down State Enable		
		RW	7	TX-Turn-off State Enable		
		RW	6	Fault State Enable		
		RW	5	Ready State Enable		
		RW	4	TX-Turn-on State Enable		
		RW	3	TX-Off State Enable		
		RW	2	High-Power-up State Enable		
		RW	1	Low-Power State Enable		
		RO	0	Initialize State Enable		
A029	1			Module General Status Enable		
		RW	15	GLB_ALRM Master Enable		
		RO	14	Reserved		
		RW	13	HW Interlock		
		RO	12~11	Reserved		
		RW	10	Loss of REFCLK Input Enable		
		RW	9	TX_JITTER_PLL_LOL Enable		
		RW	8	TX_CMU_LOL Enable		
		RW	7	TX_LOSF Enable		
		RW	6	TX_HOST_LOL Enable		
		RW	5	RX_LOS Enable		
		RW	4	RX_NETWORK_LOL Enable		
		RW	3	Out of Alignment Enable		
		RO	2~0	Reserved		
A02A	1			Module Fault Status Enable		
		RO	15~7	Reserved		
		RW	6	PLD or Flash Initialization Fault Enable		
		RW	5	Power Supply Fault Enable		
		RO	4~2	Reserved		
		RW	1	CFP Checksum Fault Enable		
A02B	1	RO		Module Alarm and Warnings 1 Enable		
			15~12	Reserved		
			11	Mod Temp Hi Alarm Enable		
			10	Mod Temp Hi Warn Enable		
			9	Mod Temp Low Warning Enable		
			8	Mod Temp Low Alarm Enable		
			7	Mod Vcc High Alarm Enable		
			6	Mod Vcc High Warning Enable		
			5	Mod Vcc Low Warning Enable		
			4	Mod Vcc Low Alarm Enable		
			3	Mod SOA Bias High Alarm Enable		
			2	Mod SOA Bias High Warning Enable		

			8	TX Power Low Alarm		
			7	Laser Temperature High Alarm		
			6	Laser Temperature High Warning		
			5	Laser Temperature Low Warning		
			4	Laser Temperature Low Alarm		
			3	RX Power High Alarm		
			2	RX Power High Warning		
			1	RX Power Low Warning		
			0	RX Power Low Alarm		
A210	16	RO		Network Lane n Fault and Status		
			15	Lane TEC Fault		
			14	Lane Wavelength Unlocked Fault		
			13	Lane APD Power Supply Fault		
			12~8	Reserved		
			7	Lane TX_LOSF		
			6	Lane TX_LOL		
			5	Reserved		
			4	Lane RX_LOS		
			3	Lane RX_LOL		
			2	Lane RX FIFO error		
			1	Reserved		
			0	Reserved		
			Network Lane FAWS Latch Registers			
A220	16	RO/LH/COR		Network Lane n Alarm and Warning Latch		
			15	Bias High Alarm Latch		
			14	Bias High Warning Latch		
			13	Bias Low Warning Latch		
			12	Bias Low Alarm Latch		
			11	TX Power High Alarm Latch		
			10	TX Power High Warning Latch		
			9	TX Power Low Warning Latch		
			8	TX Power Low Alarm Latch		
			7	Laser Temperature High Alarm Latch		
			6	Laser Temperature High Warning Latch		
			5	Laser Temperature Low Warning Latch		
			4	Laser Temperature Low Alarm Latch		
			3	RX Power High Alarm Latch		
			2	RX Power High Warning Latch		
			1	RX Power Low Warning Latch		
			0	RX Power Low Alarm Latch		
A230	16	RO/LH/COR		Network Lane n Fault and Status latch		
			15	Lane TEC Fault Latch		
			14	Lane Wavelength Unlocked Fault Latch		
			13	Lane APD Power Supply Fault Latch		
			12~8	Reserved		

			7	Lane TX_LOSF Latch		
			6	Lane TX_LOL Latch		
			5	Reserved		
			4	Lane RX_LOS Latch		
			3	Lane RX_LOL Latch		
			2	Lane RX FIFO Status Latch		
		RO	1~0	Reserved		
A240	16	RW		Network Lane n Alarm and Warning Enable		
			15	Bias High Alarm Enable		
			14	Bias High Warning Enable		
			13	Bias Low Warning Enable		
			12	Bias Low Alarm Enable		
			11	TX Power High Alarm Enable		
			10	TX Power High Warning Enable		
			9	TX Power Low Warning Enable		
			8	TX Power Low Alarm Enable		
			7	Laser Temperature High Alarm Enable		
			6	Laser Temperature High Warning Enable		
			5	Laser Temperature Low Warning Enable		
			4	Laser Temperature Low Alarm Enable		
			3	RX Power High Alarm Enable		
			2	RX Power High Warning Enable		
			1	RX Power Low Warning Enable		
A250	16		0	RX Power Low Alarm Enable		
				Network Lane n Fault and Status Enable		

A450	48	RO	15~4	Reserved		
		RW	3~0	Signal Pre/De-emphasis		
		RO		Reserved		

11	3.3V
12	3.3V
13	3.3V_GND
14	3.3V_GND
15	VND_IO_A
16	VND_IO_B
17	PRG_CNTL1
18	PRG_CNTL2
19	PRG_CNTL3
20	PRG_ALRM1
21	PRG_ALRM2
22	PRG_ALRM3
23	GND
24	TX_DIS
25	RX_LOS
26	MOD_LOPWR
27	MOD_ABS
28	MOD_RSTn
29	GLB_ALRMn
30	GND
31	MDC
32	MDIO
33	PRTADR0
34	PRTADR1
35	PRTADR2
36	VND_IO_C

94	N.C.
93	N.C.
92	GND
91	N.C.
90	N.C.
89	GND
88	TX1n
87	TX1p
86	GND
85	TX0n
84	TX0p
83	GND
82	N.C.
81	N.C.
80	GND
79	(REFCLKn)
78	(REFCLKp)
77	GND
76	N.C.
75	N.C.
74	GND
73	RX3n
72	RX3p
71	GND
70	RX2n
69	RX2p

48	N.C.
49	GND
50	(RX_MCLKn)
51	(RX_MCLKp)

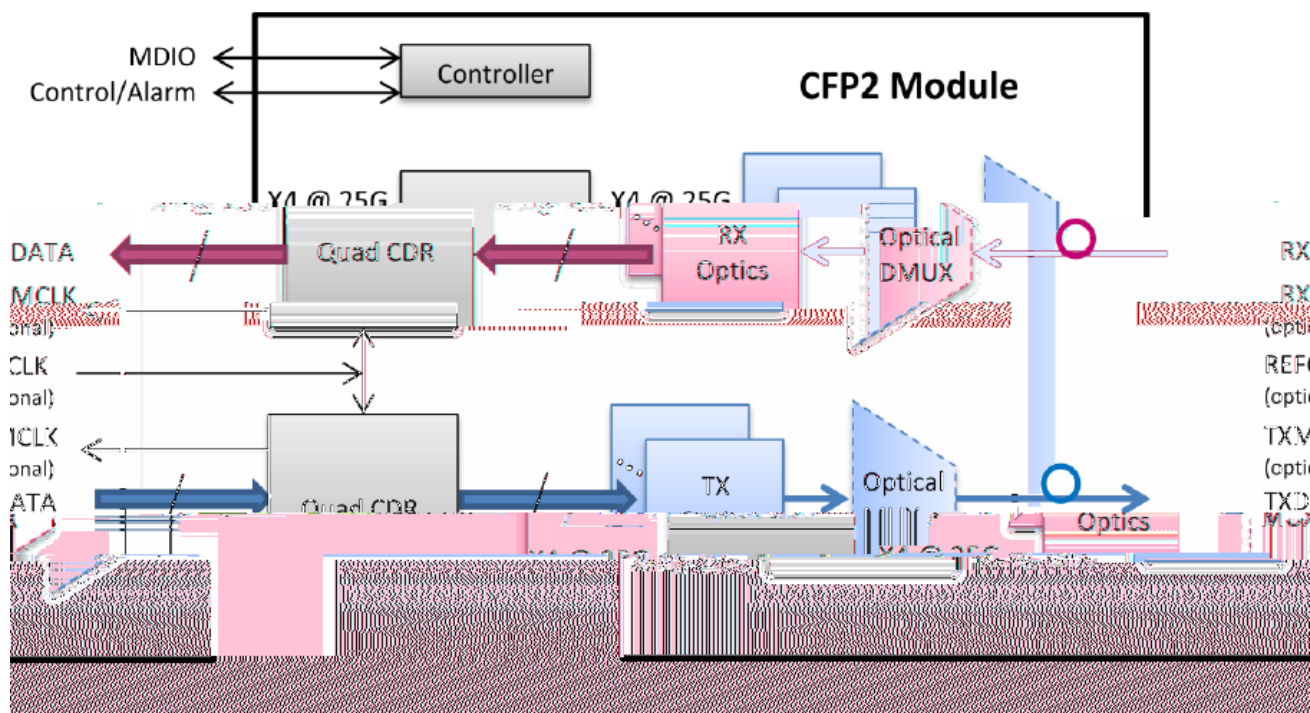
57	RX0p
56	GND
55	N.C.
54	

				signal, "0": normal condition
26	MOD_LOPWR	I	LVC MOS w/ PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled
27	MOD_ABS	O	GND	Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host
28	MOD_RSTn	I	LVC MOS w/ PDR	Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module
29	GLB_ALRMn	O	LVC MOS	Global Alarm. "0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host
30	GND			
31	MDC	I	1.2V CMOS	Management Data Clock (electrical specs as per IEEE Std 802.3-2012)
32	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per IEEE Std 802.3-2012)
33	PRTADR0	I	1.2V CMOS	MDIO Physical Port address bit 0
34	PRTADR1	I	1.2V CMOS	MDIO Physical Port address bit 1
35	PRTADR2	I	1.2V CMOS	MDIO Physical Port address bit 2
36	VND_IO_C	I/O		Module Vendor I/O C. Do Not Connect!
37	VND_IO_D	I/O		Module Vendor I/O D. Do Not Connect!
38	VND_IO_E	I/O		Module Vendor I/O E. Do Not Connect!
39	3.3V_GND			
40	3.3V_GND			
41	3.3V			3.3V Module Supply Voltage
42	3.3V			
43	3.3V			
44	3.3V			
45	3.3V_GND			
46	3.3V_GND			
47	N.C.			No Connect
48	N.C.			
49	GND			
50	(RX_MCLKn)	O	CML	For optical waveform testing. Not for normal use.
51	(RX_MCLKp)	O	CML	For optical waveform testing. Not for normal use.
52	GND			
53	GND			
54	N.C.			
55	N.C.			
56	GND			
57	RX0p	O	CML	Output Data

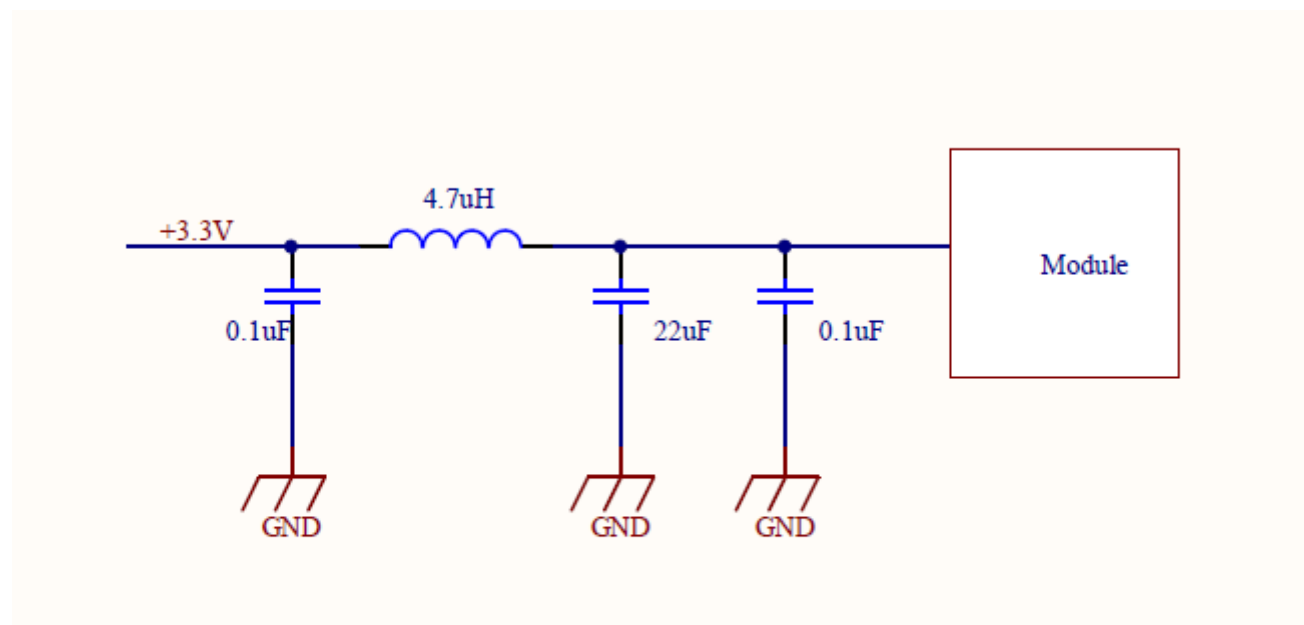
58	RX0n	O	CML	Inverted Output Data
59	GND			
60	RX1p	O	CML	Output Data
61	RX1n	O	CML	Inverted Output Data
62	GND			
63	N.C.			
64	N.C.			
65	GND			
66	N.C.			
67	N.C.			
68	GND			
69	RX2p	O	CML	Output Data
70	RX2n	O	CML	Inverted Output Data
71	GND			
72	RX3p	O	CML	Output Data
73	RX3n	O	CML	Inverted Output Data
74	GND			
75	N.C.			
76	N.C.			
77	GND			
78	(REFCLKp)			
79	(REFCLKn)			

94	N.C.			
95	GND			
96	TX2p		CML	Input Data
97	TX2n		CML	Inverted Input Data
98	GND			
99	TX3p		CML	Input Data
100	TX3n		CML	Inverted Input Data
101	GND			
102				

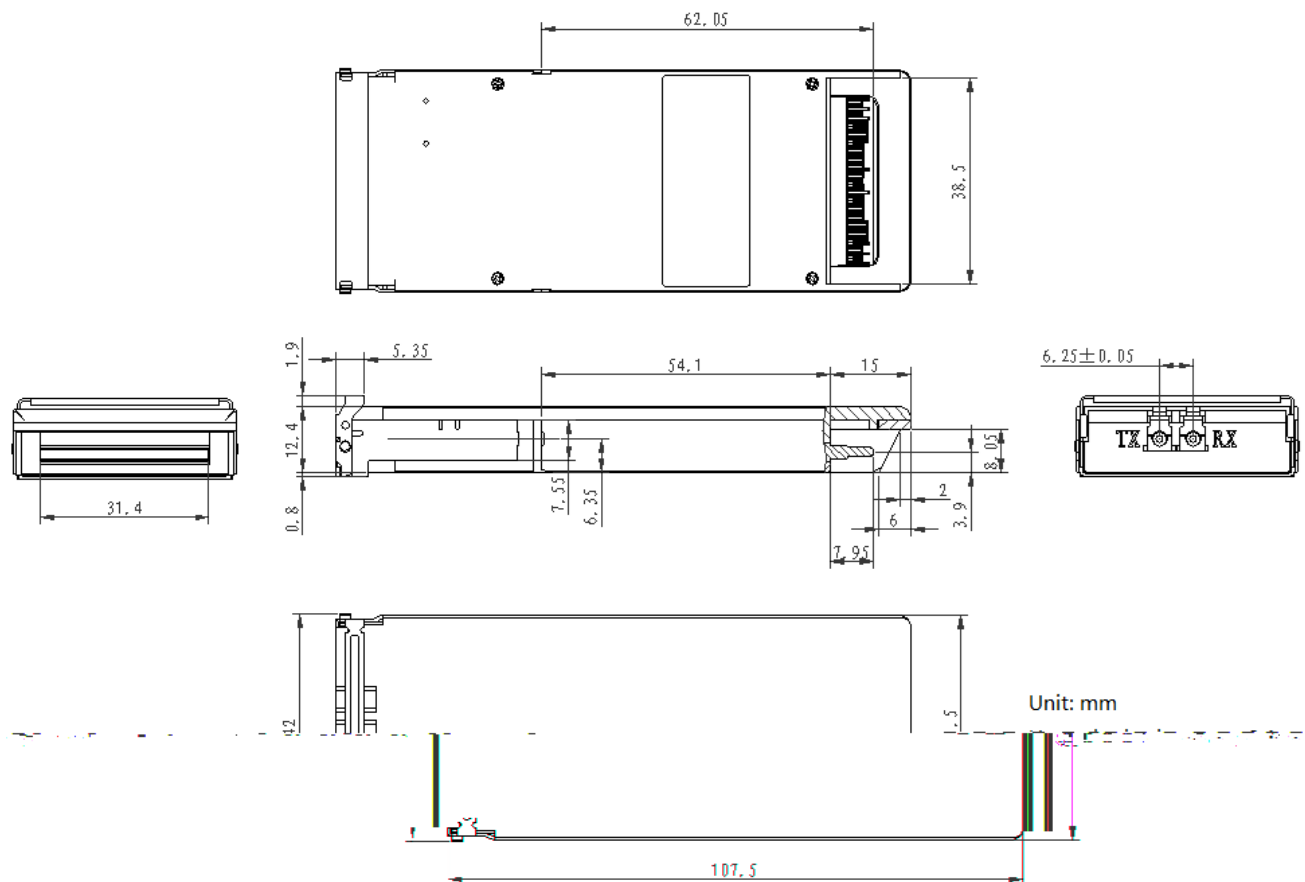
Block diagram



Required Host Board Components



Package outline



Regulatory Compliance

Feature		Test Method		Performance
Electrostatic (ESD) to the Electrical Pins	Discharge	MIL-STD-883E	JESD22-A114-B	high speed signal pins shall withstand 500V electrostatic discharge based on Human Body Model per JEDEC
		Method 3015.7	JESD22-A114-B	the other pins with exception of the high speed signal pins shall withstand 2kV electrostatic discharge based on Human Body Model per JEDEC
Electrostatic (ESD) Immunity	Discharge	IEC61000-4-2 Class B	15kV air discharges during operation and 8kV direct contact discharge	
Electromagnetic Interference (EMI)	CISPR22 ITE Class B		Compliant with standard	
	FCC Class B			
	CENELEC			
	EN55022			
	VCCI Class 1			



Immunity	IEC61000-4-3 Class 2	Compliant with any electro-magnetic regulations
Safety	FDA	
	CDRH 21-CFR 1040 Class 1	
	UL	
	TUV-GS	
	CE	

Ordering Information

Specifications

Part No