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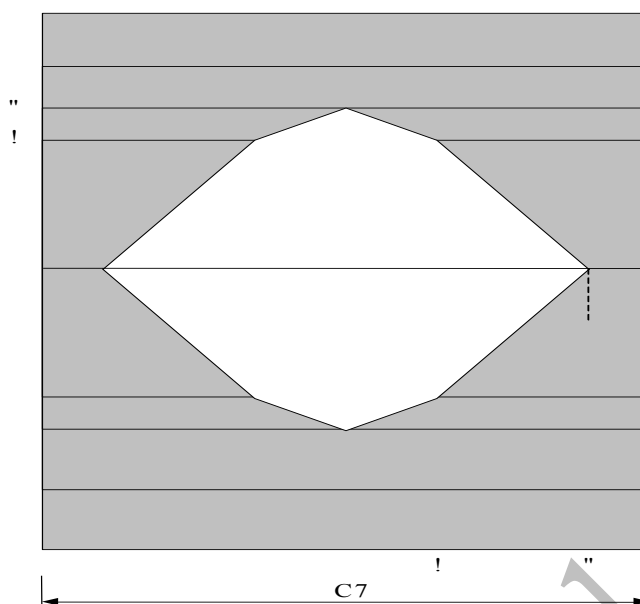


Figure 2 Mask of diagram

	155.52 Mbit/s	622.08 Mbit/s	1244.16 Mbit/s	2488.32 Mbit/s
x1/x4	0.10/0.90	0.20/0.80	0.22/0.78	For further study
x2/x3	0.35/0.65	0.40/0.60	0.40/0.60	For further study
y1/y4	0.13/0.87	0.15/0.85	0.17/0.83	For further study
y2/y3	0.20/0.80	0.20/0.80	0.20/0.80	For further study

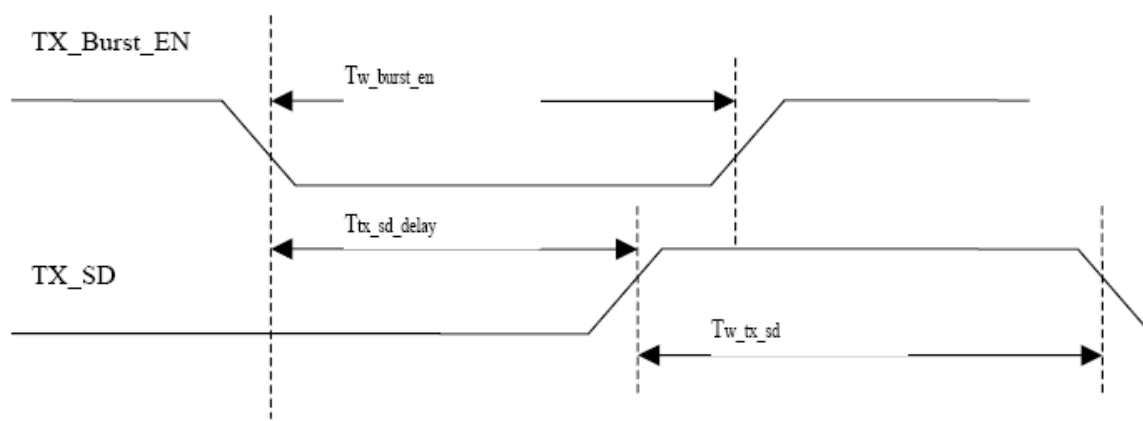
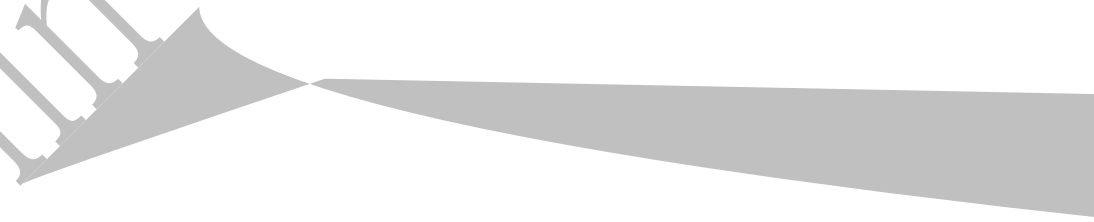


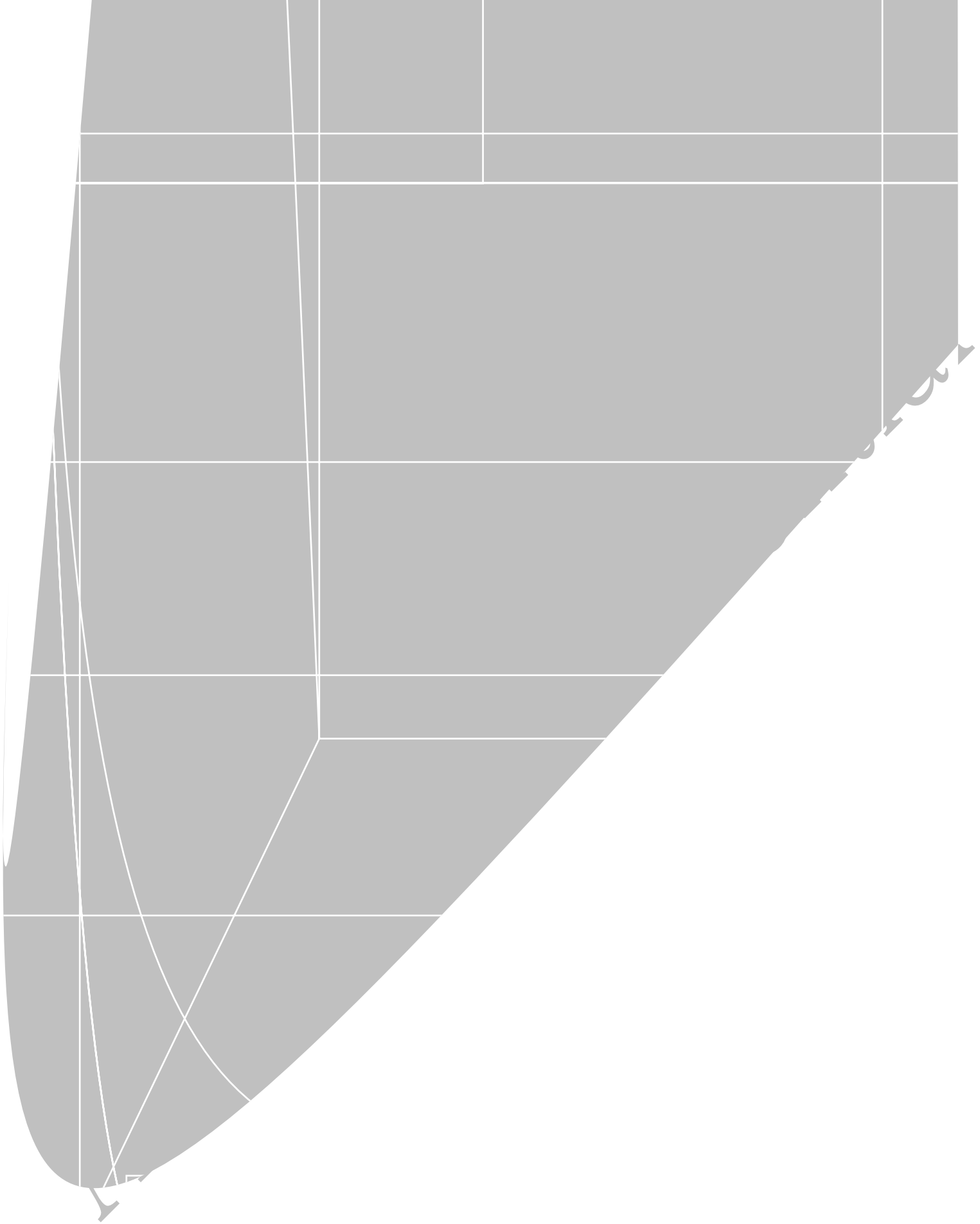
Figure 3 Timing diagram of TX_SD



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TX Power = TX Power (Digital Value) X 0.1μW

RX Power = RX Power (Digital Value) X 0.1μW

Table 2.1 Logic Status and AD Conversion Updates

Byte	Bit	Name	Description
110	7	Reserved	
110	6	Soft Tx Disable Control	1= disable, 0= enable.
110	5	Reserved	Set to 0.
110	4	Rx Rate Select State	Not supported (set to 0).
110	3	Soft Rate Select Control	Not supported (set to 0).
110	2	Tx Fault	1= fault, 0= normal.
110	1	RX-SD	1= SD, 0= LOS.
110	0	Power on Logic	Not supported (set to 0).
111	7-0	Temp A/D Valid	Not supported (set to 0).

Each of the measured values has a corresponding high alarm, low alarm, high warning and low warning threshold level at location 00-39(x0A2) written as the data format of a corresponding valued shown in Table 2.2. Alarm and warning flags at bytes 112-119(0xA2) are defined as follows.

- (1) Alarm flags indicate conditions likely to result (or have resulted) in link failure and cause for immediate action.
- (2) Warning flags indicate conditions outside the guaranteed operating specification of transceiver but not necessarily causes of immediate link failures.

Table 2.2 Alarm and Warning Flags

Byte	Bit(s)	Name	Description
112	7	Temperature High Alarm	Set when temperature monitor value exceeds high alarm level.
112	6	Temperature Low Alarm	Set when temperature monitor value exceeds low alarm level.
112	5	Vcc High Alarm	Set when Vcc monitor value exceeds high alarm level.
112	4	Vcc Low Alarm	Set when Vcc monitor value exceeds Low alarm

116	4	Vcc Low warning	Set when Vcc monitor value exceeds Low warning level.
116	3	Laser Bias High warning	Set when laser bias monitor value exceeds high warning level.
116	2	Laser Bias Low warning	Set when laser bias monitor value exceeds low warning level.
116	1	Tx Power High warning	Set when Tx power monitor value exceeds high warning level
116	0	Tx Power Low warning	Set when Tx power monitor value exceeds low warning level.
117	7	Rx Power High warning	Set when Rx power monitor value exceeds high warning level
117	6	Rx Power Low warning	Set when Rx power monitor value exceeds low warning level
117	5-0	Reserved	
118	7-0	Reserved	
119	7-0	Reserved	

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8 Block Diagram

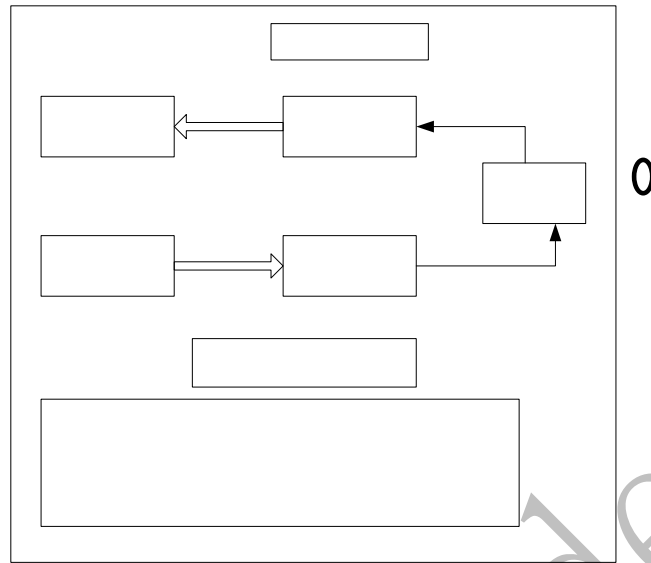
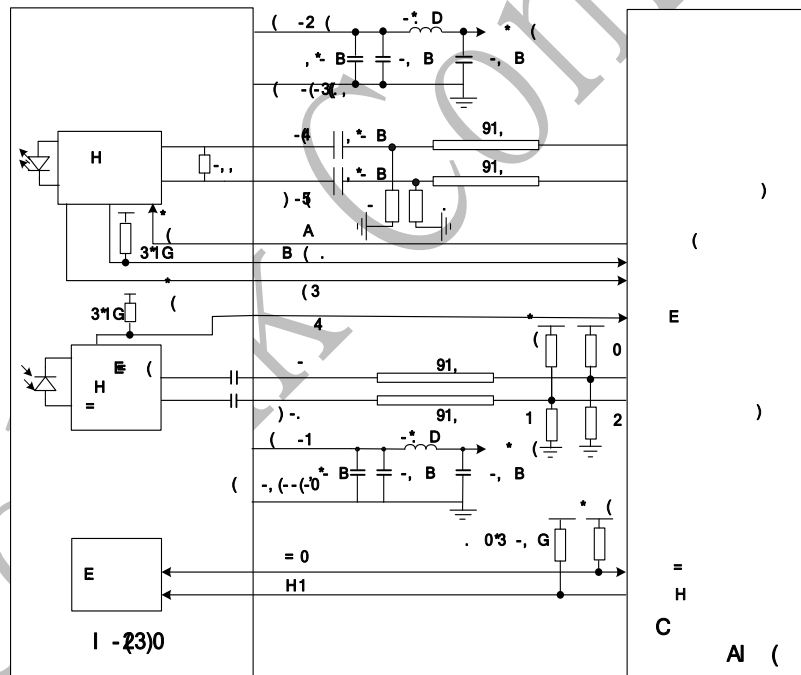


Figure 4 Functional block diagram

9 Typical Application Circuit



Note:

If output+/- in source(PON MAC IC) are CML buffer, R1,R2 can be omitted.

If input+/- in source(PON MAC IC) are CML buffer, R3,R4,R5,R6 can be omitted.

Default both are LVPECL.

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